

Model Name : IG41M-M7S
Marketing name : G41D3+
VER: 6.1

CPU :
Intel Core 2 Quad /Core 2 Duo/
Pentium Dual-Core /Celeron Dual Core /Celeron 4xx
System Chipset :

Intel G41
Intel ICH7

On Board Chip :

Clock Gen. -- RTM876-665 SSOP 56P
Azalia Codec -- RealTek ALC662-GR
GigaBit Lan -- RealTek RTL8111DL/8102EL
PWM Controller -- UP6219 QFP48
Super I/O -- IT8721FBX
SPI Flash 8Mb

Main Memory :

2 Channel DDR 3 * 2 (Max 4GB)

Expansion Slot :

PCI Express x16 Slot * 1
PCI Slot * 2

Heatsink :

NB: SBLS-T
SB: BNP SMALL-L


I/O Pannel :

47-RIOBRACKET-68

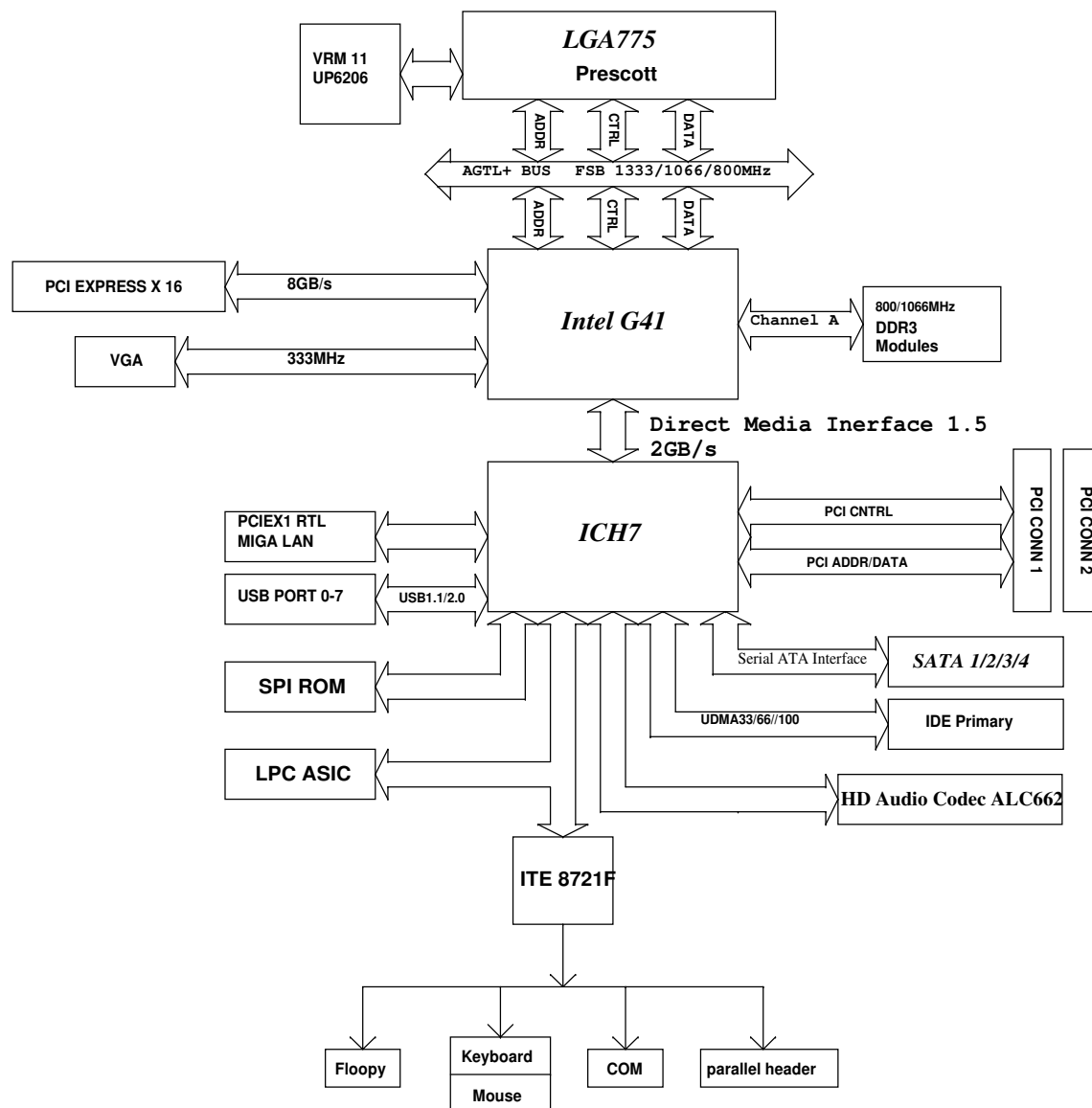
PCB SIZE :

182.05*235.00mm
4-layers-1080

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HW Engineer:		Date:	
HW Leader:		Date:	
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BLOCK DIAGRAM



PCI SLOT	IDE SEL	INT#	GNT#	REQ#	CLOCK
SLOT 1	AD17	A	0	0	PCLK_SLOT0
SLOT 2	AD18	B	1	1	PCLK_SLOT1

SUPERIO	GP NUM	TYPE	POWER	FUNCTION
PIN3	GP64	DIOD8	VCC5	EXTERNAL_PSI#
PIN13	GP35	DIOD8	VCC5	CHIP_OV_CTL
PIN18	GP31	DIOD8	VCC5	MCHREFSEL0
PIN19	GP30	DIOD8	VCC5	MCHREFSEL1
PIN20	GP27	DIOD8	VCC5	VCHIP0
PIN21	GP26	DIOD8	VCC5	VCHIP1
PIN22	GP25	DIOD8	VCC5	VTT_FSB_VHT0
PIN23	GP24	DIOD8	VCC5	VTT_FSB_VHT1
PIN24	GP23	DIOD8	VCC5	OVCPU_CORE0
PIN25	GP22	DIOD8	VCC5	OVCPU_CORE1
PIN26	GP21	DIOD8	VCC5	VDIMM2
PIN27	GP20	DIOD8	VCC5	VDIMM1
PIN28	GP17	DIOD8	VCC5	DDR_OV_CTL
PIN29	GP16	DIOD8	VCC5	VDIMM0
PIN66	GP47	DIOD8	VCC5	THERMAL#
PIN77	GP53	DIOD8	VCCH	IO_LED2
PIN78	GP41	DIOD8	VCCH	WATCH_DOG

IG41E-M7S V0.6

CPU:

Intel Core 2 Duo / Quad / Extreme, Celeron 4xx, Pentium
Dual-Core, Celeron Dual-core (FSB1600/1333/1066/800) 95W
3-Phase Power

SYSTEM CHIP:

Intel ICH7 (South Bridge)
Intel EaglelakeG41-A3 GMCH (North Bridge)

ONBOARD CHIP:

SUPERIO: ITE8721FX
AUDIO CODE: ALC662 5.1Channel Audio
LAN CHIP: Realtek RTL8103EL
CLOCK GEN:RTM876-665
DDR/CHIP PWM: FP6321A
DDR VTT: FP6137E

MEMORY SPEC:

DDR3 1200(OC)*2 /1333/1066/800
MAX 4G DUAL CHANNEL

CPU PWM:


PWM: UP6206 3PHASE UP1 LOW1 95W
COLAY UP1 LOW2

PCB SIZE

uATX,182.0mmx235.0mm, 4-Layer

EXPANSION SLOTS:

1x PCIEX16 SLOT;
2x PCI SLOT;
1x IDE connector;
1x FLOPPY connector;
4x SATA connectors;
1x CPU Fan header;
1x System Fan Header;
1 x Front Panel Header;
1 x Front Panel Audio Header;
1 x Serial Port Header;
8 x USB 2.0/1.1 Headers

 映泰股份有限公司 BIOSSTAR GROUP	
Title: GENERAL SPEC	
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1. 2010/06/18 COLAY 1000M LAN, ADD BURN IN SOLUTION(U7.5)

V6.1

- 2010/11/15
- 1

modify for support FSB533MHz and Memory 1333MHZ
Remove R264,R14,R16,R49,Q1,Q2
R18 change to 10K
R17.2 connect to +3V3_DUAL, R17 reserved
R18.1 connect to BSEL2C,R18 reserved
Q3.D connect to MCH_BSEL2, Q3 and Q4 reserved
R369 reserved
RN3 change to single res
Remove R285,Q74
- 2

PR14.1,PR25.1 and R170.2 connect to VCC12QQ,PD4/PD5 --> VCC12QQ
- 3

R243,R249 change to 2.7 ohm, add R244,R251,C229/C234 change to 4.7uF
- 4

All E-CAP colay
- 5

Add RN41,RN42
- 6

Add AQ2,AQ6
- 7

Add PC49
- 8

remove LCT1,add LC20,LC21
- 9

Q45 AND Q46 value changed ,LAN ESD
- 10

Remove RN33 ,add R172,R173
- 11

Remove LINE2 VREF
- 12

NI AC19
- 13

RN45 change to 4 res(R305,R308,R309,R310)
- 14

FB19 value change to inductor
- 15

R492.1 connect to VCC5
- 16

Remove SR35,SR37,SR39,SR40
- 17

add CT18
- 18

Remove ATX POWERGD LEVEL SHIFT
- 19

Remove PSI control circuit
- 20

Add SC23
- 21

Add R100
- 22

SRN11 change to 4 res
- 23

RN46 swap net

Eaglelake G41 Strap Pins:(Collected By Tonylee 08/03)

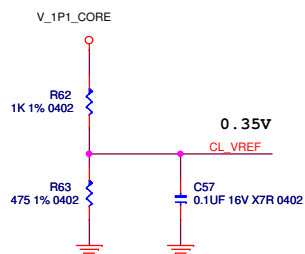
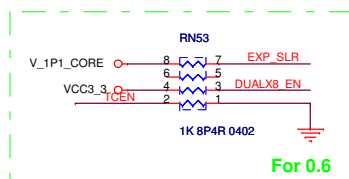
ITPM_ENB[L17]
0 = Enable Intel TPM
1 = Disable Intel TPM

DualX8_Enable[F20](Input)
0 = 2x8 PCI Express Ports Enabled
1 = 1x16 PCI Express Port Enabled

CEN[J17](Input)
0 = Disable TLS
1 = Enable TLS

EXP_SLR[F15]
0 = (G)MCH PCI Express lane numbers are reversed (BTX)
1 = Normal operation (ATX)

EXP_SM[H17](Input)
0 = Only SDVO or PCI Express is operational.HDA&HDMI are reserved for Heil card.
1 = Both SDVO and PCI Express are operating simultaneously via the PCI Express port.

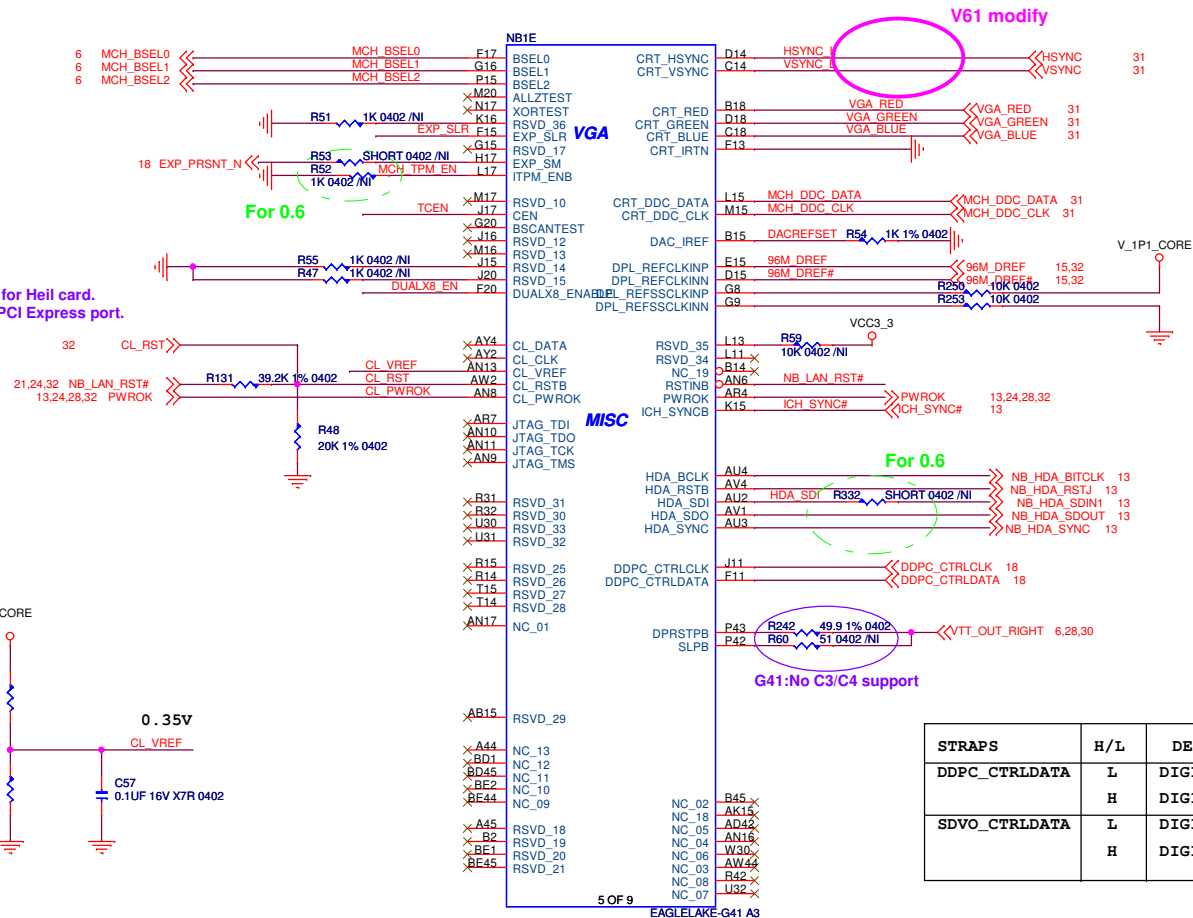


For 0.6

6 MCH_BSEL2 << R286 0 0402 >> MCH_BSEL2_C 24

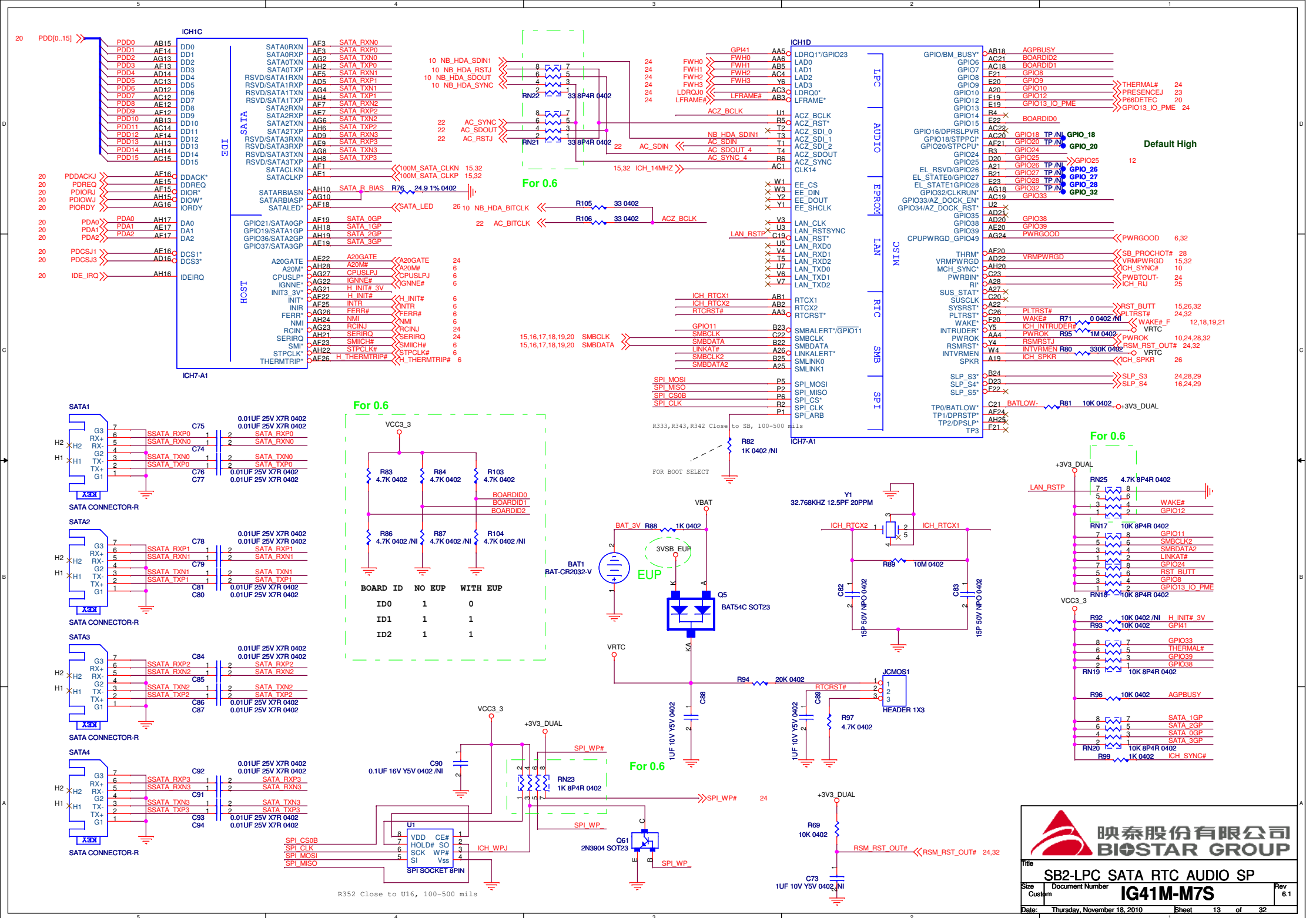
MODIFY V6.1

SUPPORT 1333MHz memory



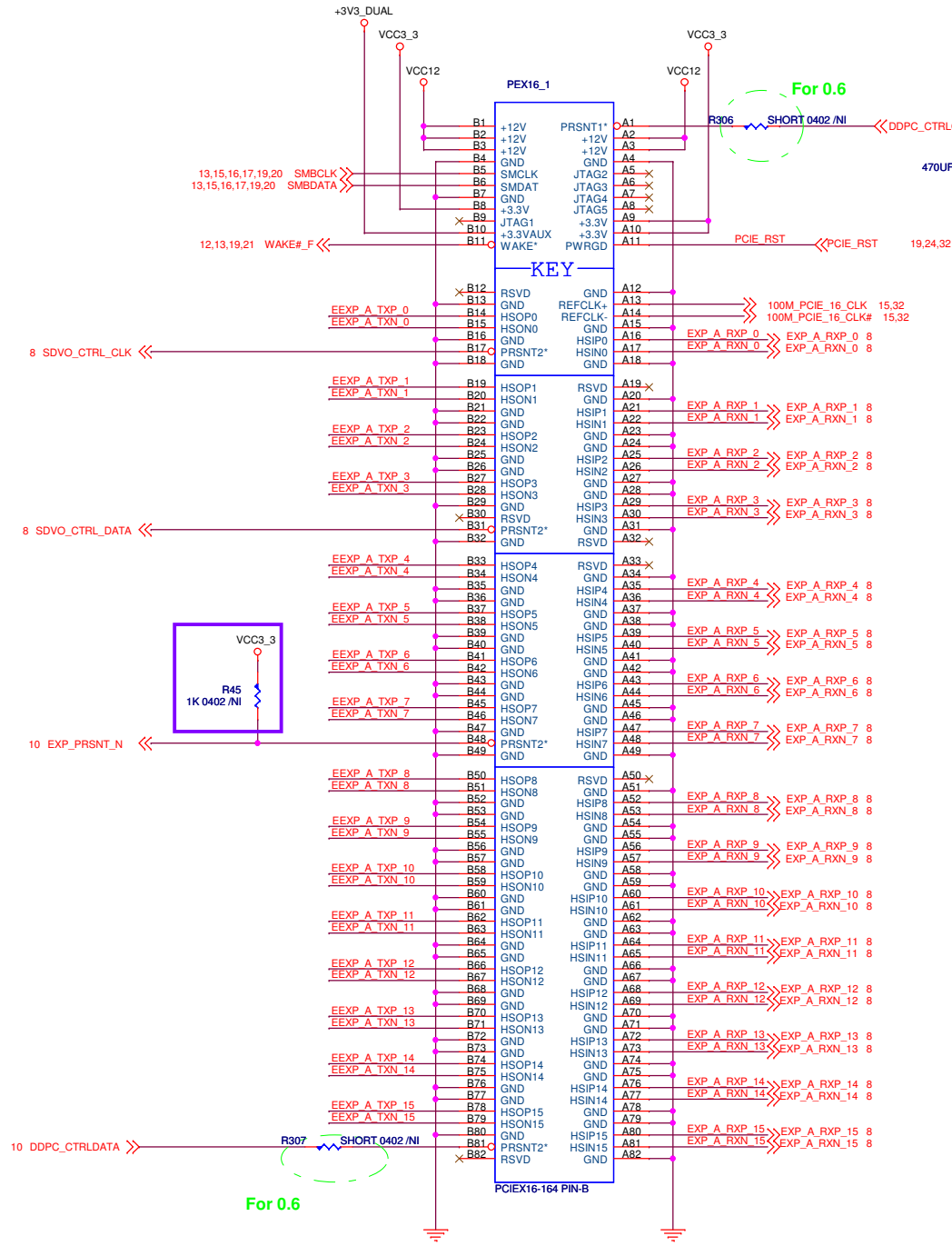
STRAPS	H/L	DESCRIPTION
DDPC_CTRLDATA	L	DIGITAL DISPLAY PORT C DISABLE
	H	DIGITAL DISPLAY PORT C ENABLE
SDVO_CTRLDATA	L	DIGITAL DISPLAY PORT B DISABLE
	H	DIGITAL DISPLAY PORT B ENABLE



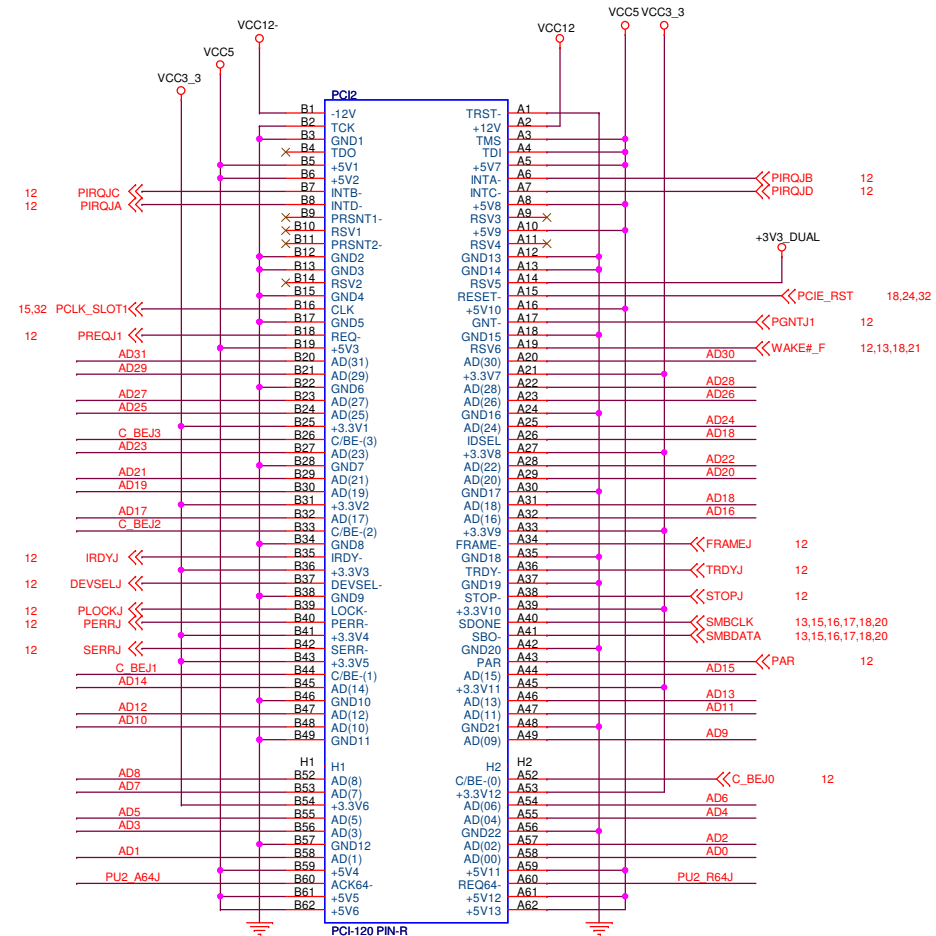
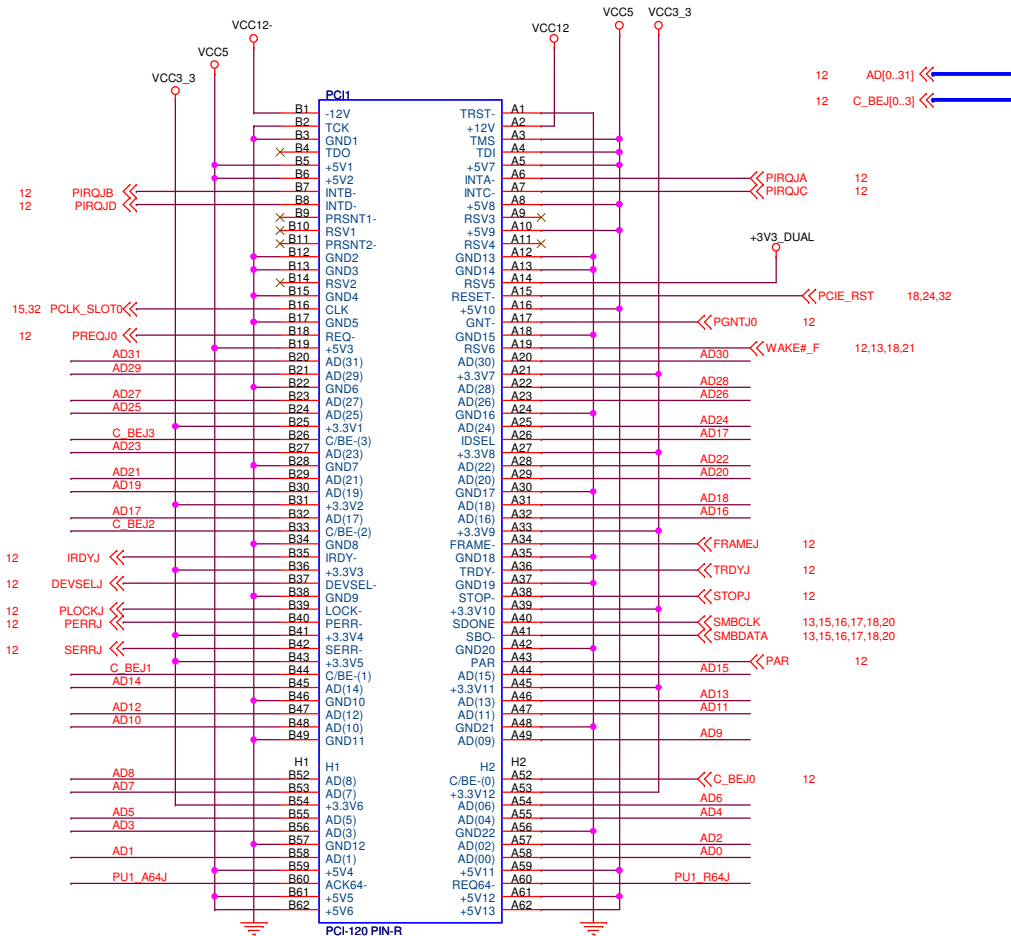


Title			
SB2-LPC SATA RTC AUDIO SP			
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8 EXP_A_TXP_0 << EXP_A_TXP_0_1 2 EEXP_A_TXP_0
C160 0.1UF 16V X7R 0402
8 EXP_A_TXN_0 << EXP_A_TXN_0_1 2 EEXP_A_TXN_0
C161 0.1UF 16V X7R 0402
8 EXP_A_TXP_1 << EXP_A_TXP_1_1 2 EEXP_A_TXP_1
C162 0.1UF 16V X7R 0402
8 EXP_A_TXN_1 << EXP_A_TXN_1_1 2 EEXP_A_TXN_1
C163 0.1UF 16V X7R 0402
8 EXP_A_TXP_2 << EXP_A_TXP_2_1 2 EEXP_A_TXP_2
C164 0.1UF 16V X7R 0402
8 EXP_A_TXN_2 << EXP_A_TXN_2_1 2 EEXP_A_TXN_2
C165 0.1UF 16V X7R 0402
8 EXP_A_TXP_3 << EXP_A_TXP_3_1 2 EEXP_A_TXP_3
C166 0.1UF 16V X7R 0402
8 EXP_A_TXN_3 << EXP_A_TXN_3_1 2 EEXP_A_TXN_3
C167 0.1UF 16V X7R 0402
8 EXP_A_TXP_4 << EXP_A_TXP_4_1 2 EEXP_A_TXP_4
C168 0.1UF 16V X7R 0402
8 EXP_A_TXN_4 << EXP_A_TXN_4_1 2 EEXP_A_TXN_4
C169 0.1UF 16V X7R 0402
8 EXP_A_TXP_5 << EXP_A_TXP_5_1 2 EEXP_A_TXP_5
C170 0.1UF 16V X7R 0402
8 EXP_A_TXN_5 << EXP_A_TXN_5_1 2 EEXP_A_TXN_5
C171 0.1UF 16V X7R 0402
8 EXP_A_TXP_6 << EXP_A_TXP_6_1 2 EEXP_A_TXP_6
C172 0.1UF 16V X7R 0402
8 EXP_A_TXN_6 << EXP_A_TXN_6_1 2 EEXP_A_TXN_6
C173 0.1UF 16V X7R 0402
8 EXP_A_TXP_7 << EXP_A_TXP_7_1 2 EEXP_A_TXP_7
C174 0.1UF 16V X7R 0402
8 EXP_A_TXN_7 << EXP_A_TXN_7_1 2 EEXP_A_TXN_7
C175 0.1UF 16V X7R 0402
8 EXP_A_TXP_8 << EXP_A_TXP_8_1 2 EEXP_A_TXP_8
C176 0.1UF 16V X7R 0402
8 EXP_A_TXN_8 << EXP_A_TXN_8_1 2 EEXP_A_TXN_8
C177 0.1UF 16V X7R 0402
8 EXP_A_TXP_9 << EXP_A_TXP_9_1 2 EEXP_A_TXP_9
C178 0.1UF 16V X7R 0402
8 EXP_A_TXN_9 << EXP_A_TXN_9_1 2 EEXP_A_TXN_9
C179 0.1UF 16V X7R 0402
8 EXP_A_TXP_10 << EXP_A_TXP_10_1 2 EEXP_A_TXP_10
C180 0.1UF 16V X7R 0402
8 EXP_A_TXN_10 << EXP_A_TXN_10_1 2 EEXP_A_TXN_10
C181 0.1UF 16V X7R 0402
8 EXP_A_TXP_11 << EXP_A_TXP_11_1 2 EEXP_A_TXP_11
C182 0.1UF 16V X7R 0402
8 EXP_A_TXN_11 << EXP_A_TXN_11_1 2 EEXP_A_TXN_11
C183 0.1UF 16V X7R 0402
8 EXP_A_TXP_12 << EXP_A_TXP_12_1 2 EEXP_A_TXP_12
C184 0.1UF 16V X7R 0402
8 EXP_A_TXN_12 << EXP_A_TXN_12_1 2 EEXP_A_TXN_12
C185 0.1UF 16V X7R 0402
8 EXP_A_TXP_13 << EXP_A_TXP_13_1 2 EEXP_A_TXP_13
C186 0.1UF 16V X7R 0402
8 EXP_A_TXN_13 << EXP_A_TXN_13_1 2 EEXP_A_TXN_13
C187 0.1UF 16V X7R 0402
8 EXP_A_TXP_14 << EXP_A_TXP_14_1 2 EEXP_A_TXP_14
C188 0.1UF 16V X7R 0402
8 EXP_A_TXN_14 << EXP_A_TXN_14_1 2 EEXP_A_TXN_14
C189 0.1UF 16V X7R 0402
8 EXP_A_TXP_15 << EXP_A_TXP_15_1 2 EEXP_A_TXP_15
C190 0.1UF 16V X7R 0402
8 EXP_A_TXN_15 << EXP_A_TXN_15_1 2 EEXP_A_TXN_15
C191 0.1UF 16V X7R 0402



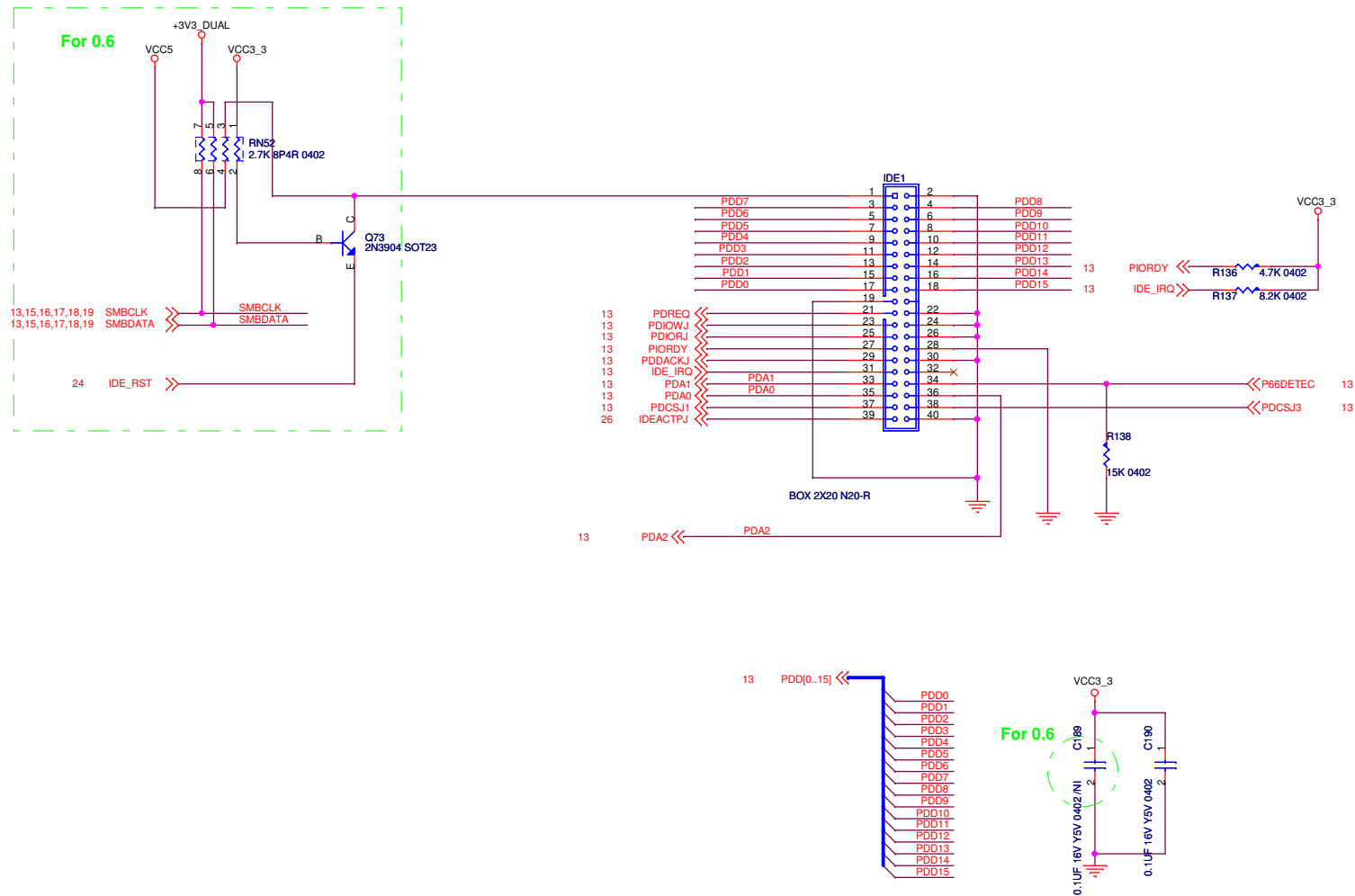
PEX16 SLOT CURRENT
VCC12---->5A
VCC3_3---->3A
+3V3_DUAL---->0.375A(S0)
0.02A(S3)



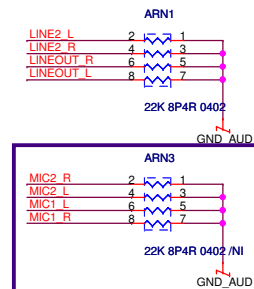
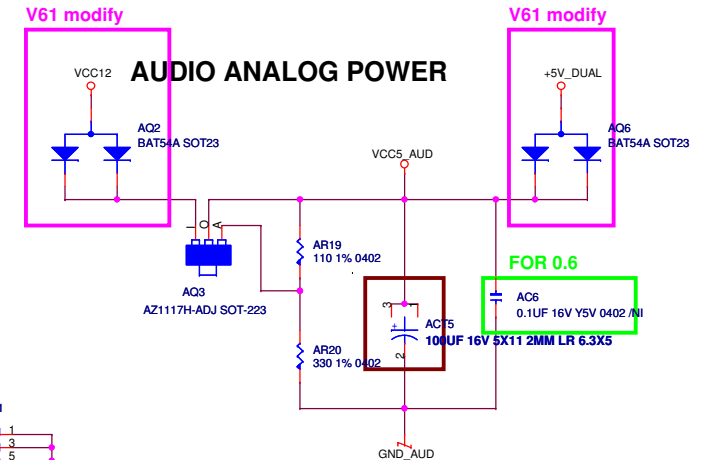
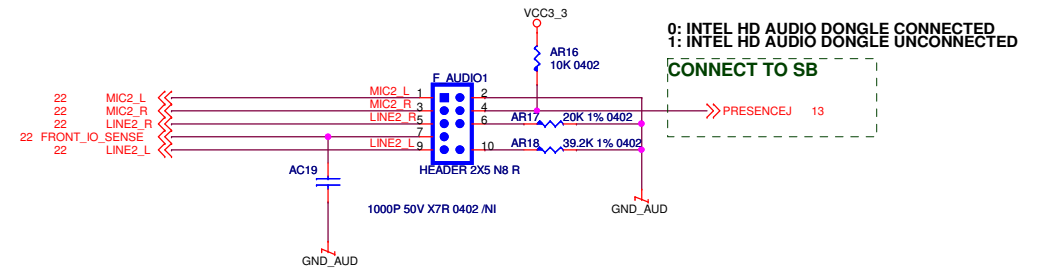
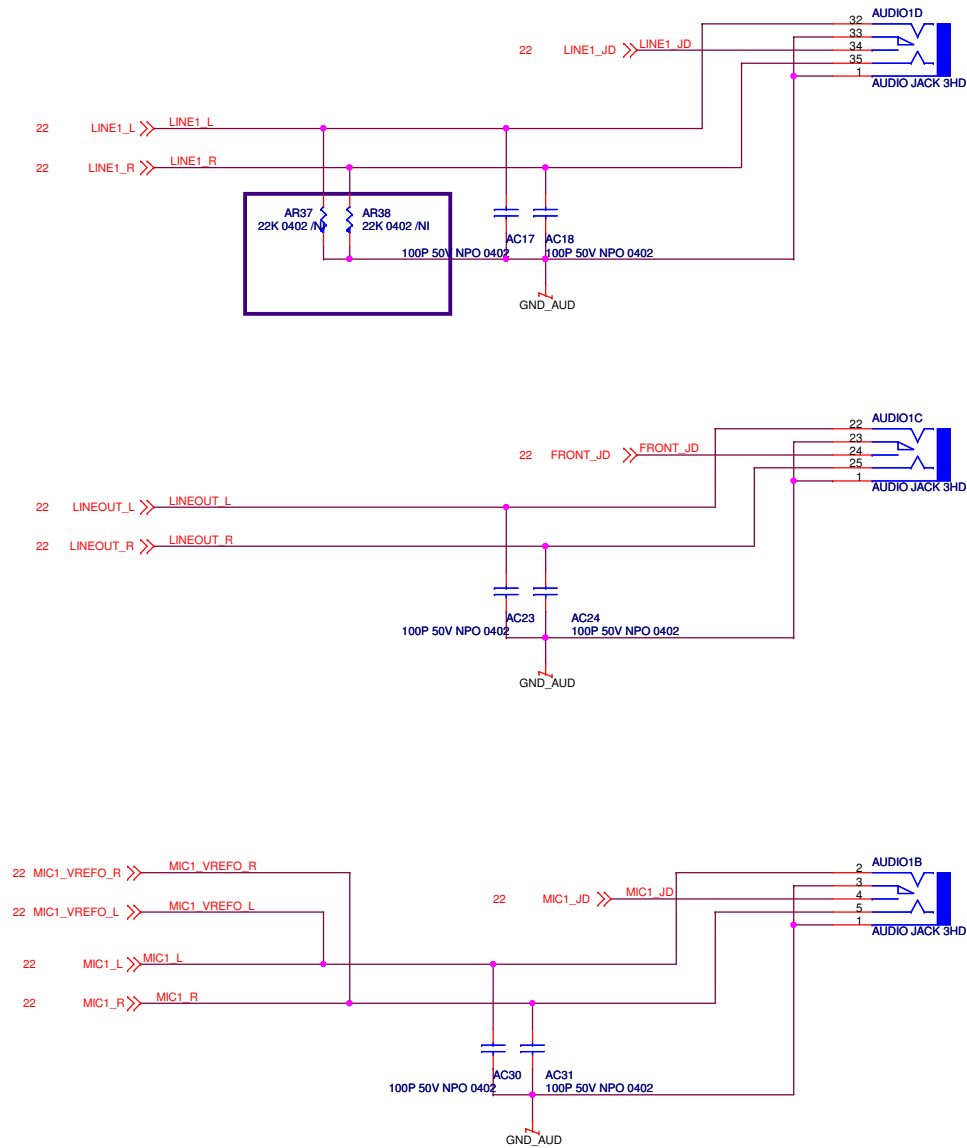
PCI SLOTS CURRENT
VCC5---->5A
VCC3_3---->7.6A
+3V3_DUAL---->0.375A(S0)/0.02A(S3)
VCC12---->0.5A
-VCC12---->0.1A

	PCI SLOT 1	PCI SLOT 2
PCICLK	PCLK_SLOT0	PCLK_SLOT1
INTR	ABCD	BCDA
IDSEL	AD17	AD18

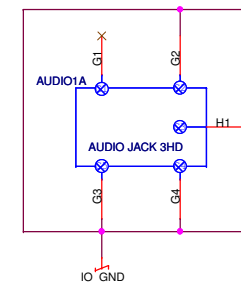


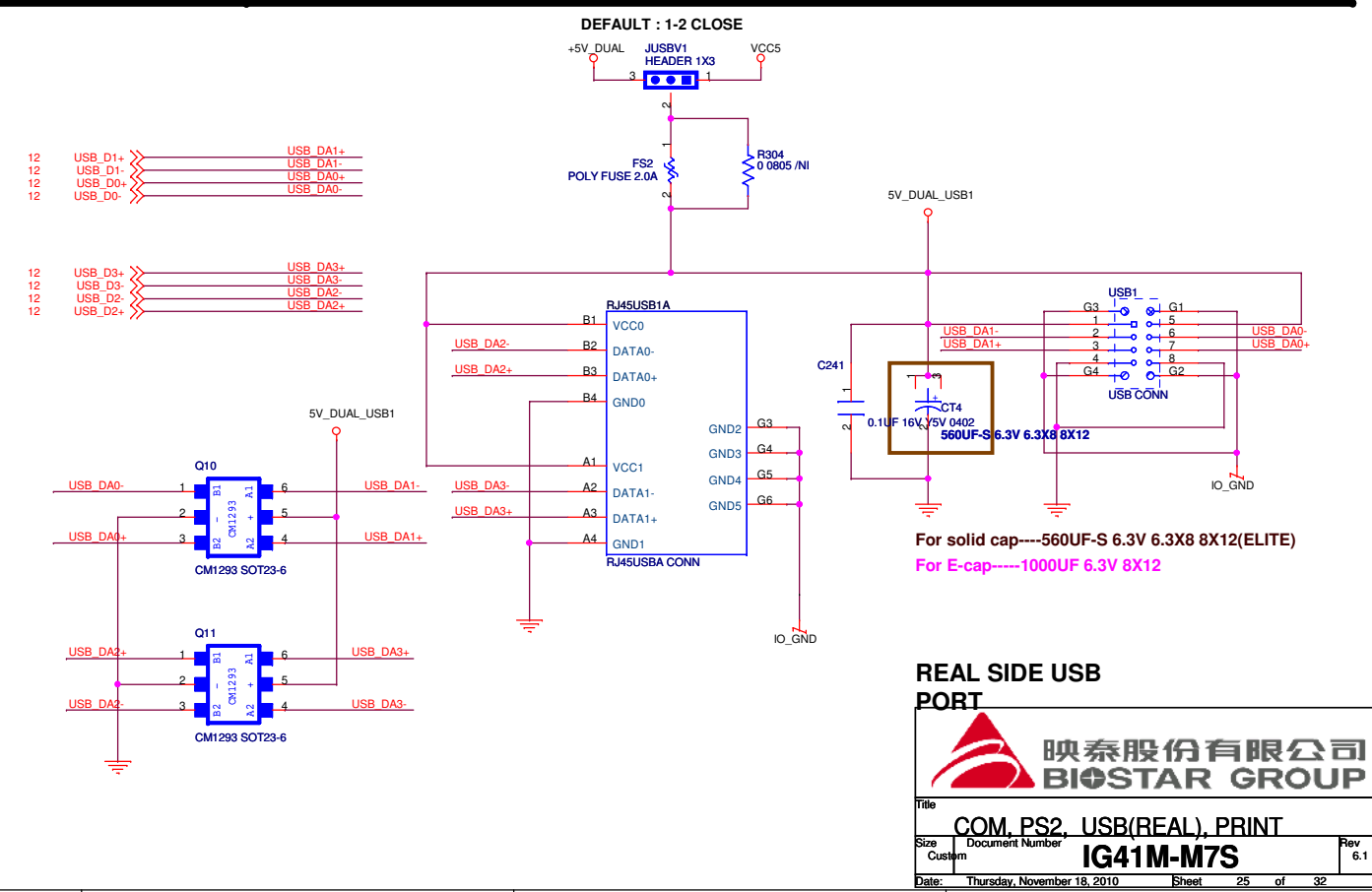
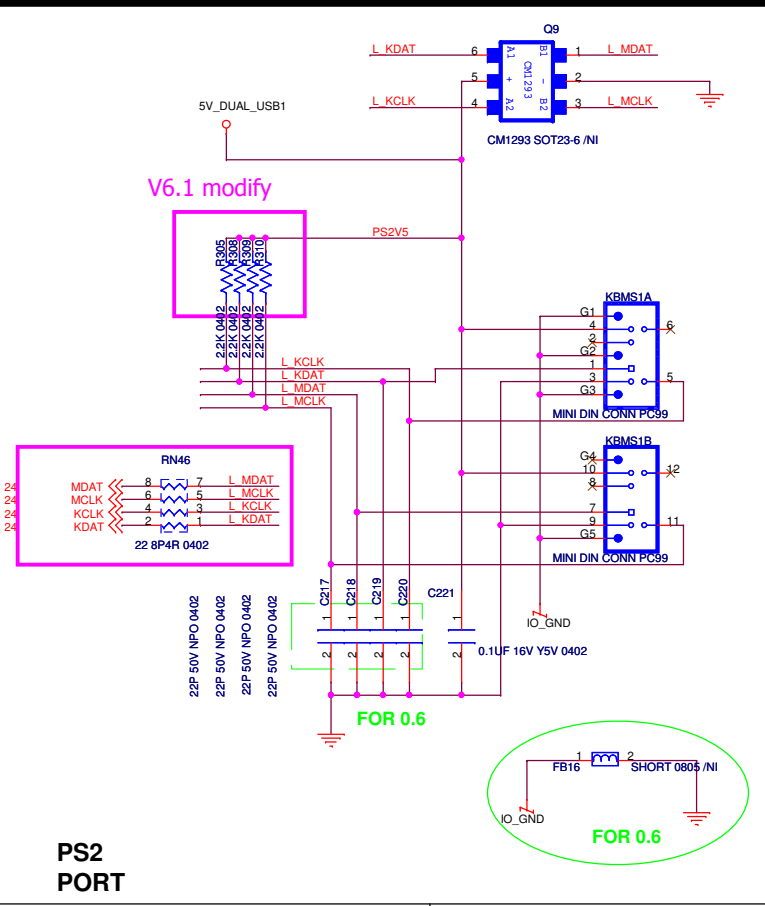
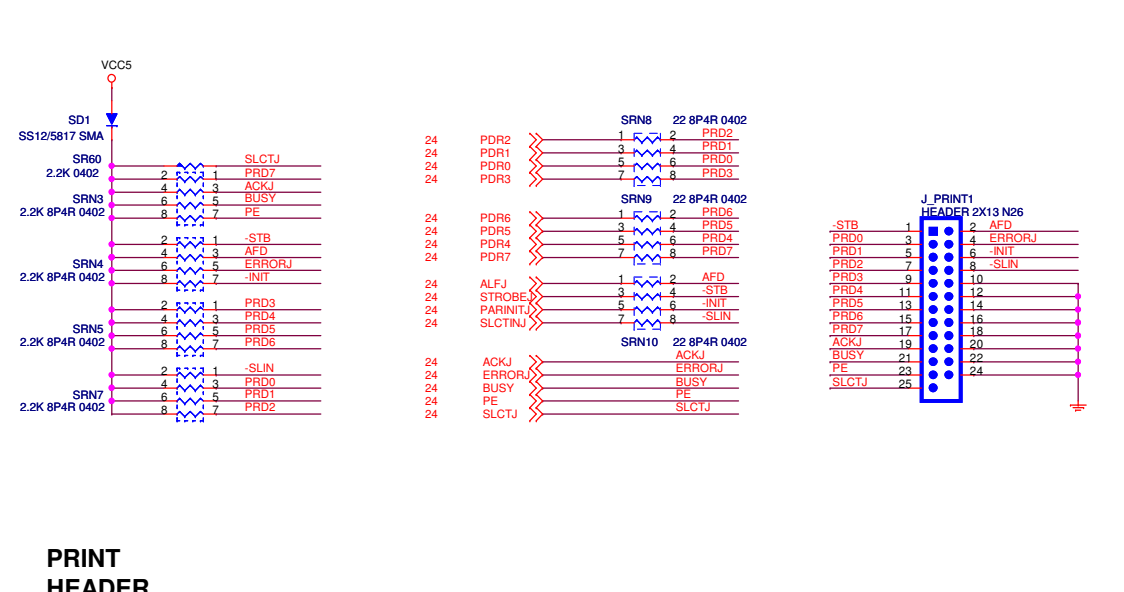
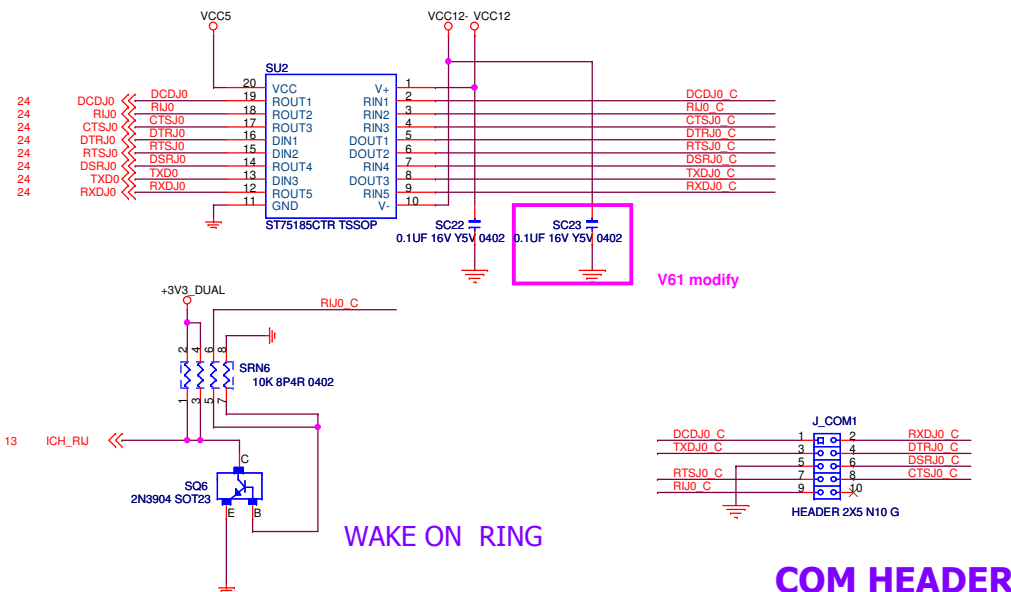


Rear Panel Onboard Analog I/O



NETIN: 100UF 16V 5X11 2MM LR 6.3X5
BOM: 100UF 16V 5X11 2mm LR
100UF-S 16V 6.3X8 ELITE





REAL SIDE USB PORT

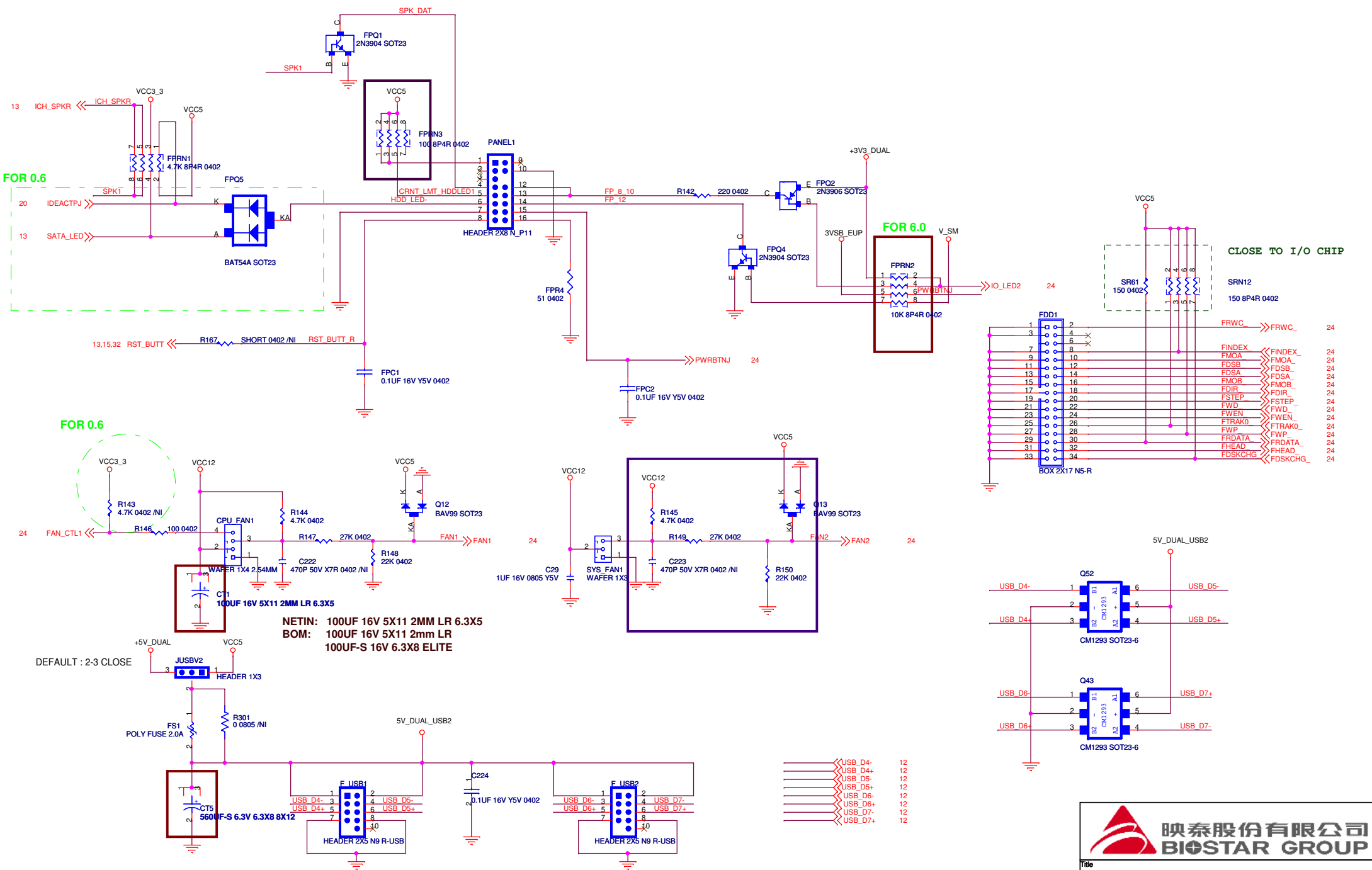
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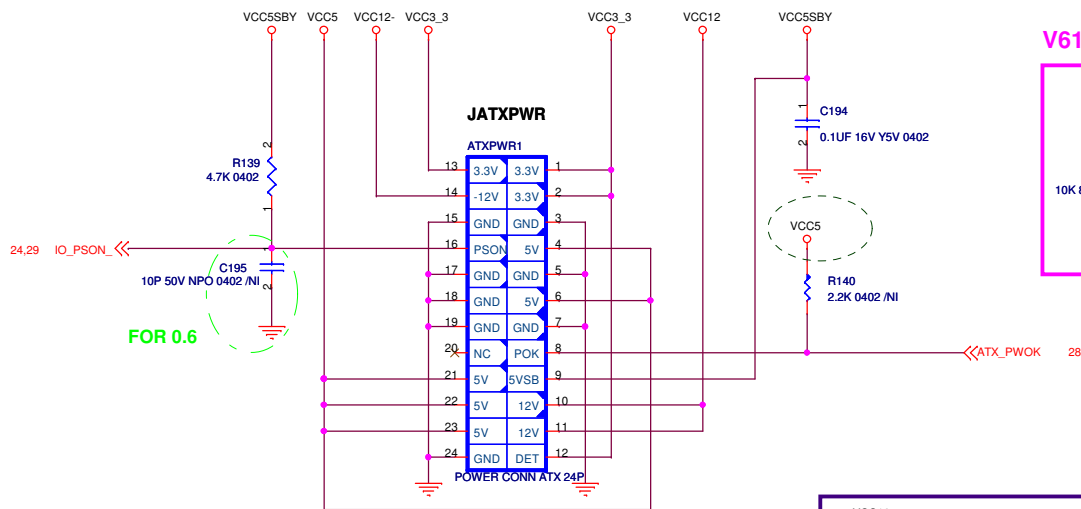
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Size: **IG41M-M7S**

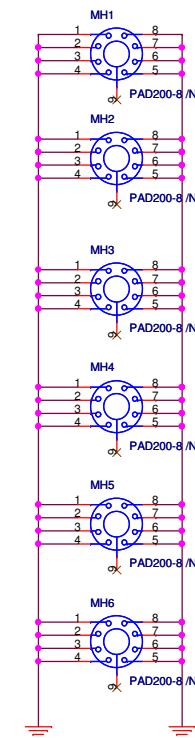
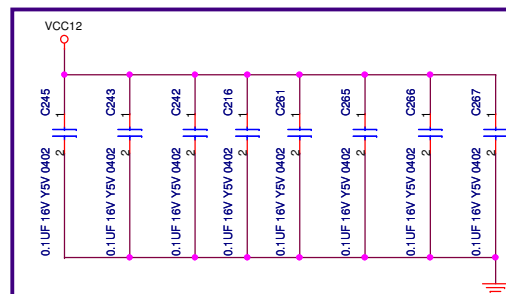
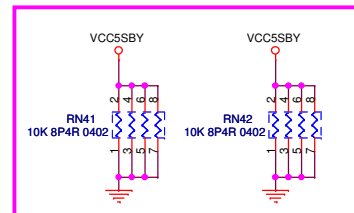
Customer: **IG41M-M7S**

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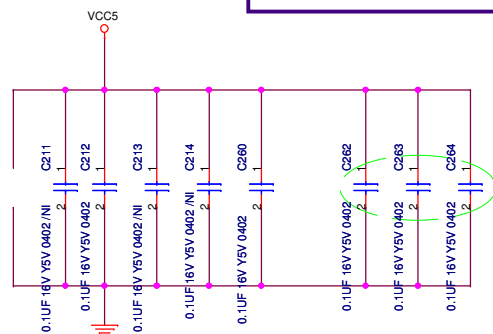
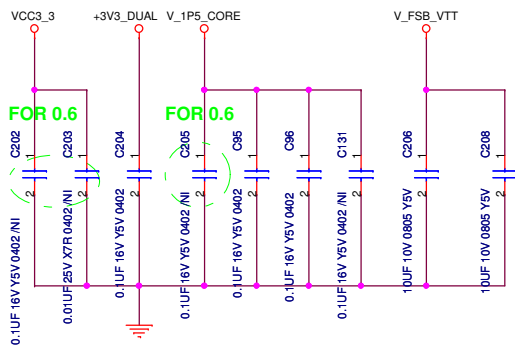
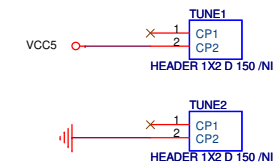




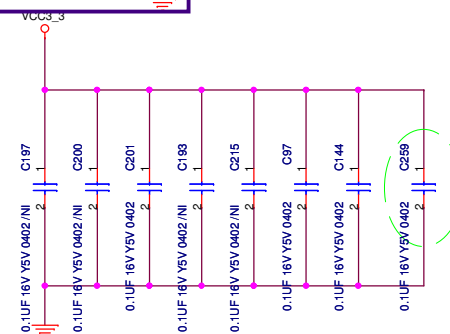
V61 modify



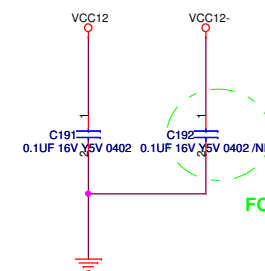
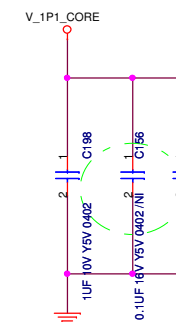
Impedance Testing Coupon

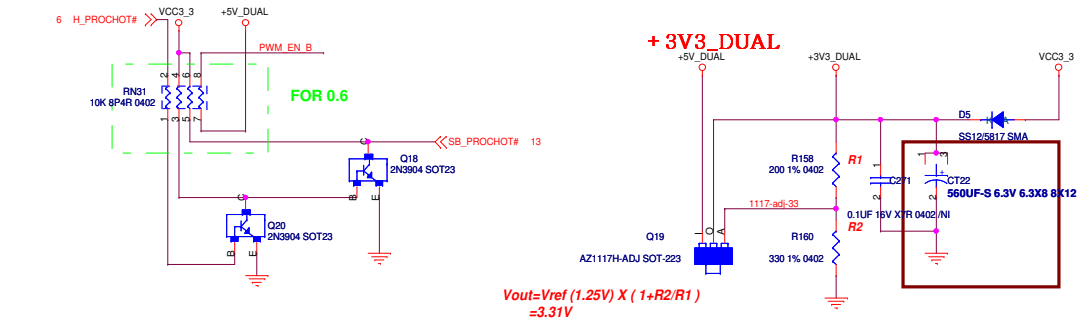


C262 close to AC18 For EMI
C263 close to LC1 For EMI
C264 close to RN36 For EMI
C265 close to LC1 For EMI

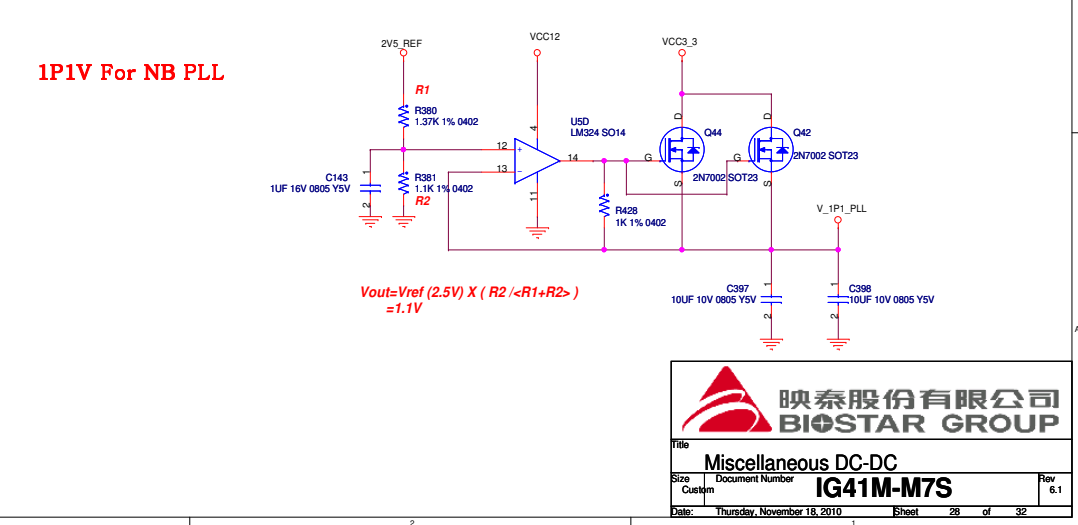
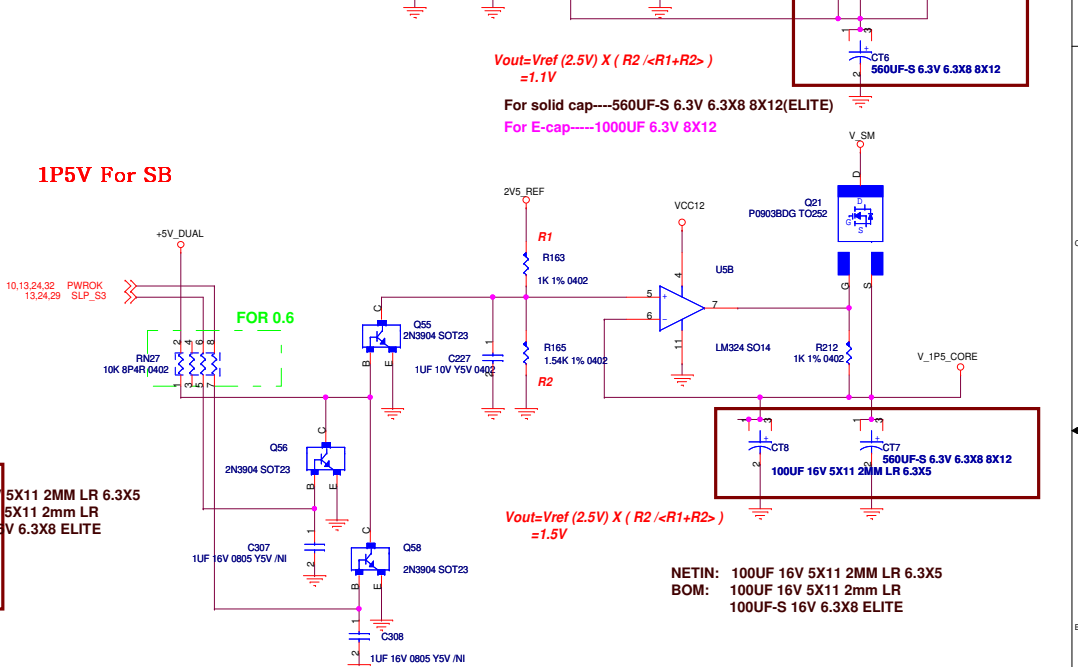
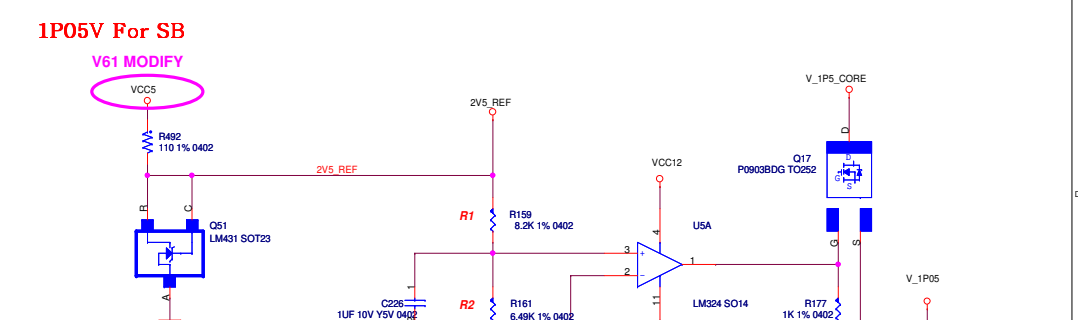
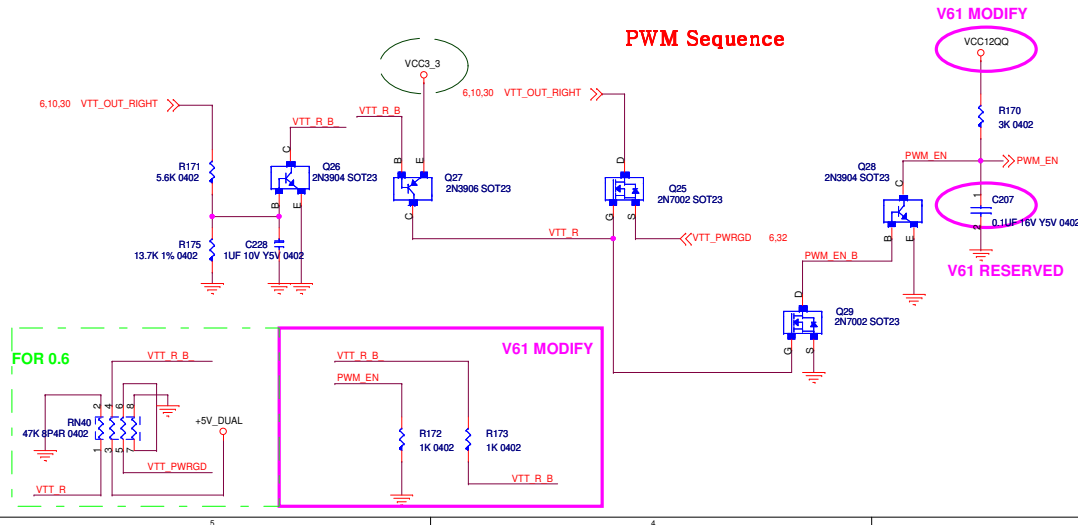
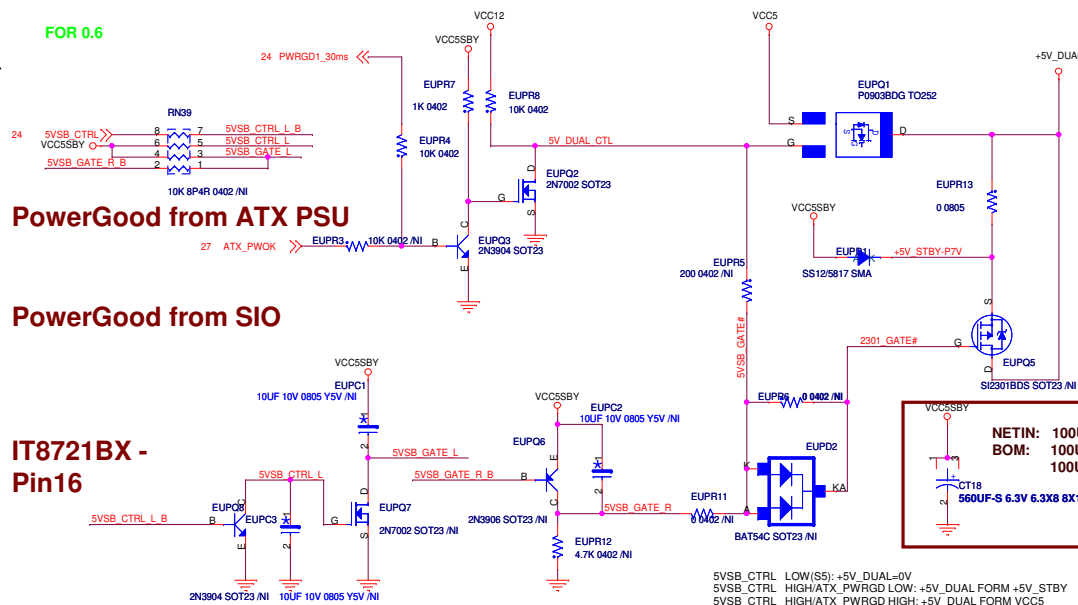


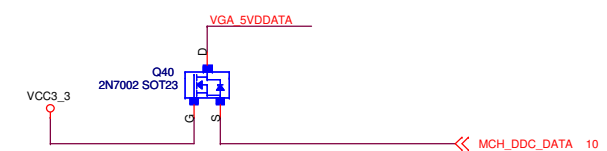
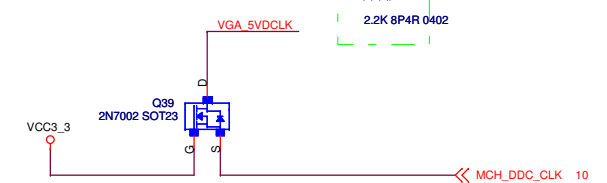
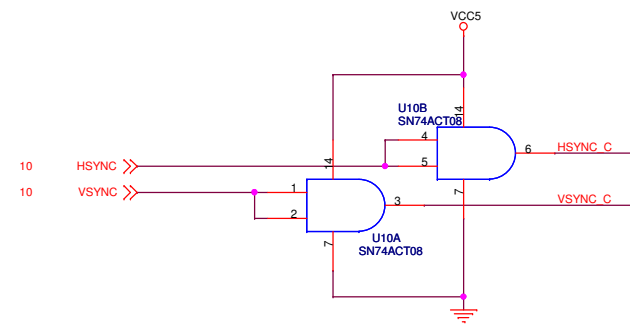
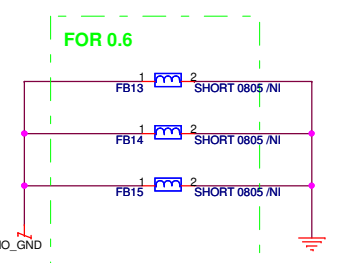
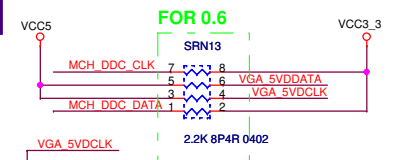
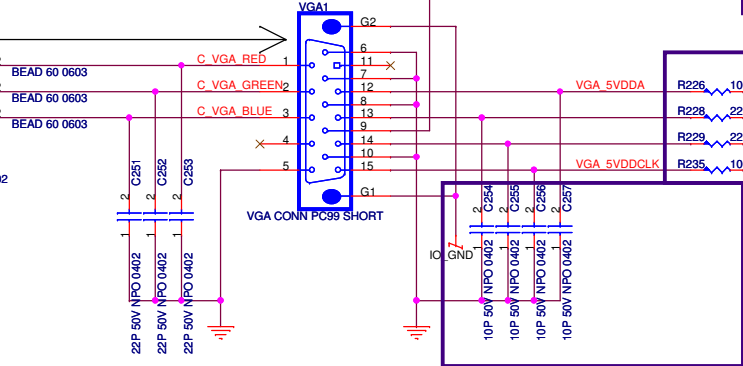
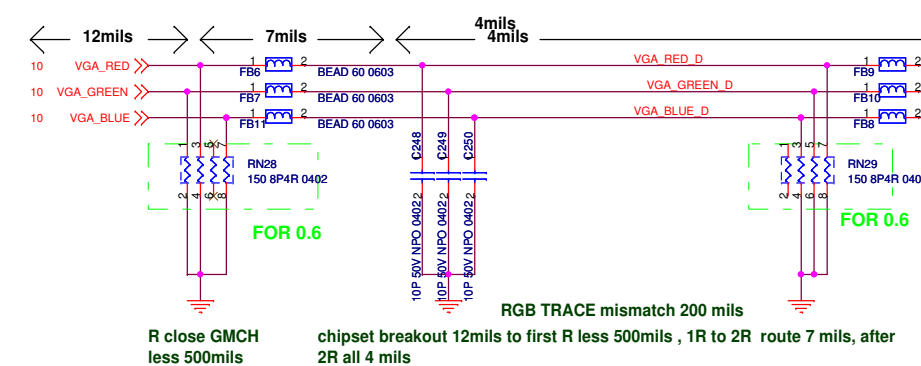
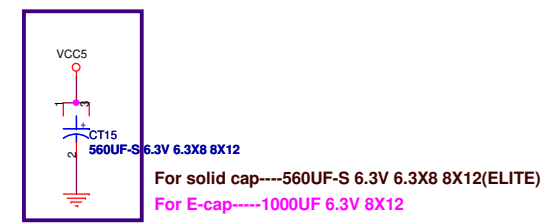
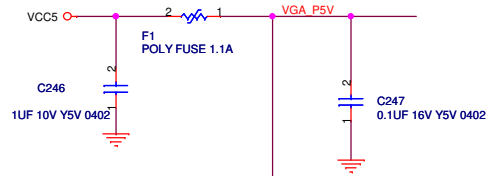
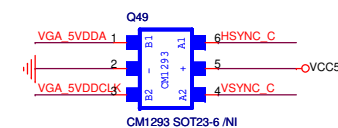
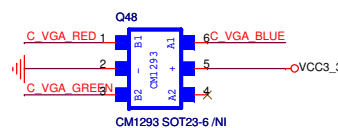
Place Close To R297 For EMI



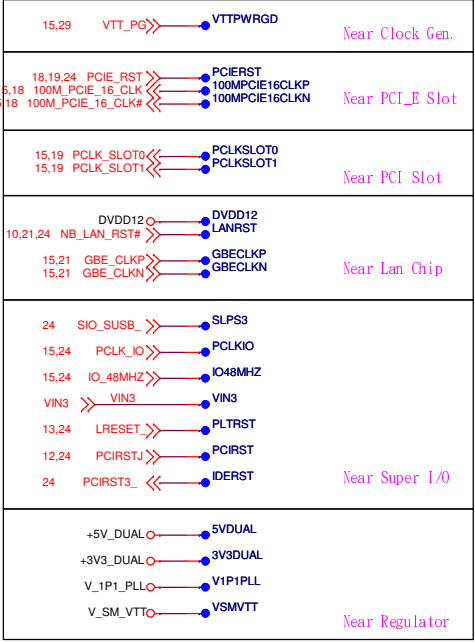
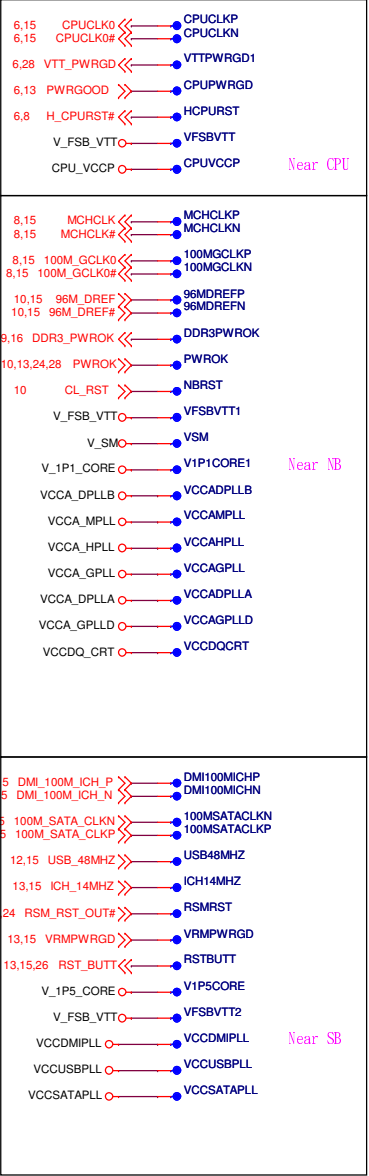
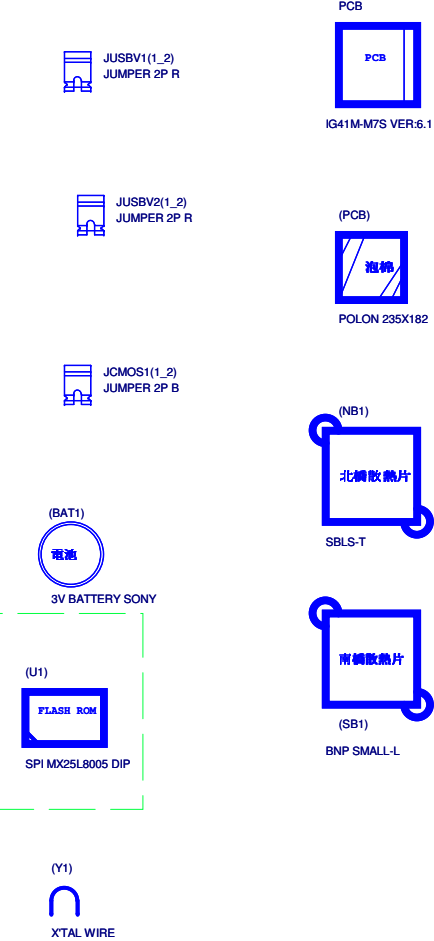


Energy-Using Product(EUP) + 5V_DUAL






Testing Point for Socket775
platform



G41M-M7S v:0.61, IG41N-M7S v:0.61 EMI Solution

崎樓cap GND_AUD to GND C262 需
AR15 剩 104pf ?

15-N31-160000R11 ... IG41M-M7S VER:6.0 需 OSP+塞(182.05*235.00*1.5)mm 4L ?
86-IG41MM7S-R01P-60
96-IG41MM7S-R01P-60



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